AMENDMENT OF SPECIFICATION

Please replace the first paragraph at original page 12, lines 1 to 13, with the following amended paragraph:

The [Processing] processing details of the trench etch are as follows :[[.]] The film stack is comprised of a bi-layer hard mask termed, Top HM1, and Bottom HM2, and a inter-metal dielectric layer, IMD, under the bilayer hard mask. Therefore, [[The]] the combination of HM1/ HM2/ IMD stack ~~[[, inter-metal dielectric~~]] consists of, which can be any one of these schemes:

HM1	HM2	[[~~IMD~~]]	IMD
USG/	SiC or SiN/	Fluorine doped Oxide or	SiO_2
USG/	SiC /	Carbon-doped Oxide	
USG/	SiC /	Organic based low-k dielectric	
USG/	SiC /	porous low-k dielectric	

(Note: [[~~where~~]] USG, is undoped silicate glass for the HM1 layer, hard mask top layer, and can also [[can]] be a conventional $Si0_2$ film of thickness in the range from 1000 to 2000 Angstroms .)

Please replace the second paragraph at original page 15, lines 15 to 21, with the following amended paragraph:

For completeness, the following is a detailed reactive ion etch, RIE, processing scheme for trench etch making use of the advantages of the bi-layer hard mask. This serves as just one example that was developed and reduced to practice, for RIE gas mixtures comprised of:

Step 1: CF_4 [[/]] and Ar based for etching [[BARC]] opening in the BARC, the bottom antireflection coating

Step 2: CF_4 [[/]] and CHF_3 [[/]] with Ar [[based]] for etching through the HM1, the top hard mask layer [[etch]]

Step 3: N_2 [[/]] and O_2 [[based]] for etching the via-fill material recess

Step 4: CF_4 [[/]] and N_2 [[/]] with O_2 [[based]] for etching the HM2, the bottom hard mask layer, and the IMD, inter-metal dielectric [[etch]]

Step 5: O_2 [[based]] for Ashing

Step 6: CHF_3 [[/]] with N_2 [[based]] for bottom etch stop layer etch